Kolloquium zur Masterarbeit

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***„X-In-The-Loop Testing of ARINC 653
Partitions Using Flight Gear "***

Embedded solutions have been developing rapidly in recent years in all sectors. The use of systems-on-chip (SoCs), which combine multiple processor cores in a single device is becoming popular in a variety of application areas: telephony, aeronautics, automotive, and so on. With them come increasingly rapid development needs, which are very demanding in terms of quality. Traditionally conservative industries, such as aerospace, are showing strong interest in multi-core processors, forcing system designers to reconsider their reliability constraints. This thesis investigates the use of flight simulations as test environments to verify the partitioning of avionics systems in general, and multi-core avionics systems in particular.

Freitag, 25.11.2022, 10:00 Uhr

Videokonferenz: BBB https://webconf.tu-clausthal.de/b/jor-a6p-een